

FIG. 1

150, 151A, 151B, 151C, 151D, 151E, 151F, 151G, 152A, 152B, 152C, 152D, 152E, 152F, 153, 154, 155

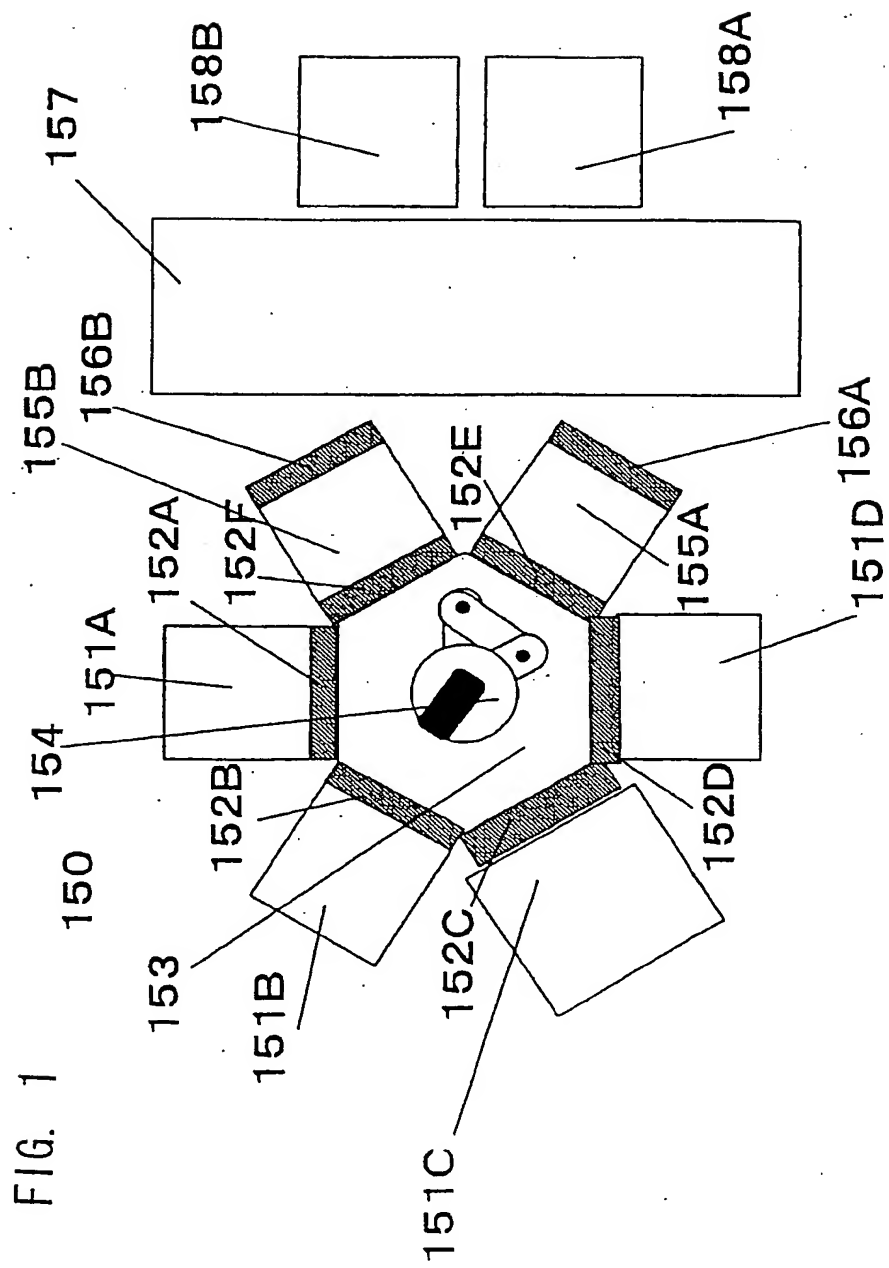


FIG 2

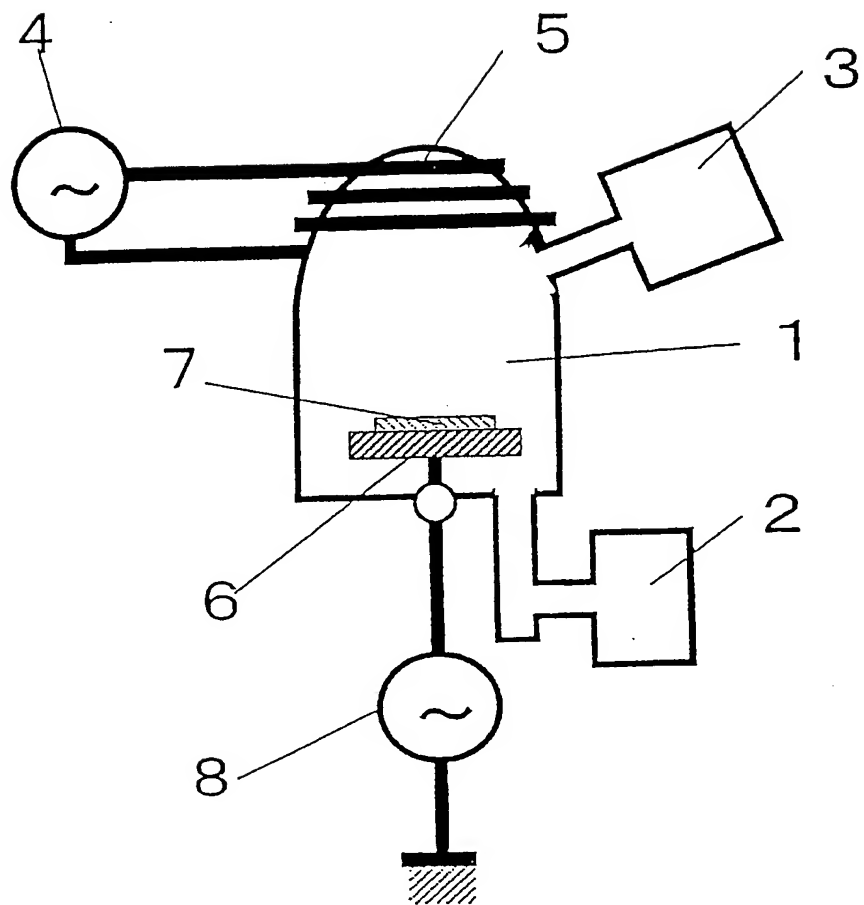


FIG. 3

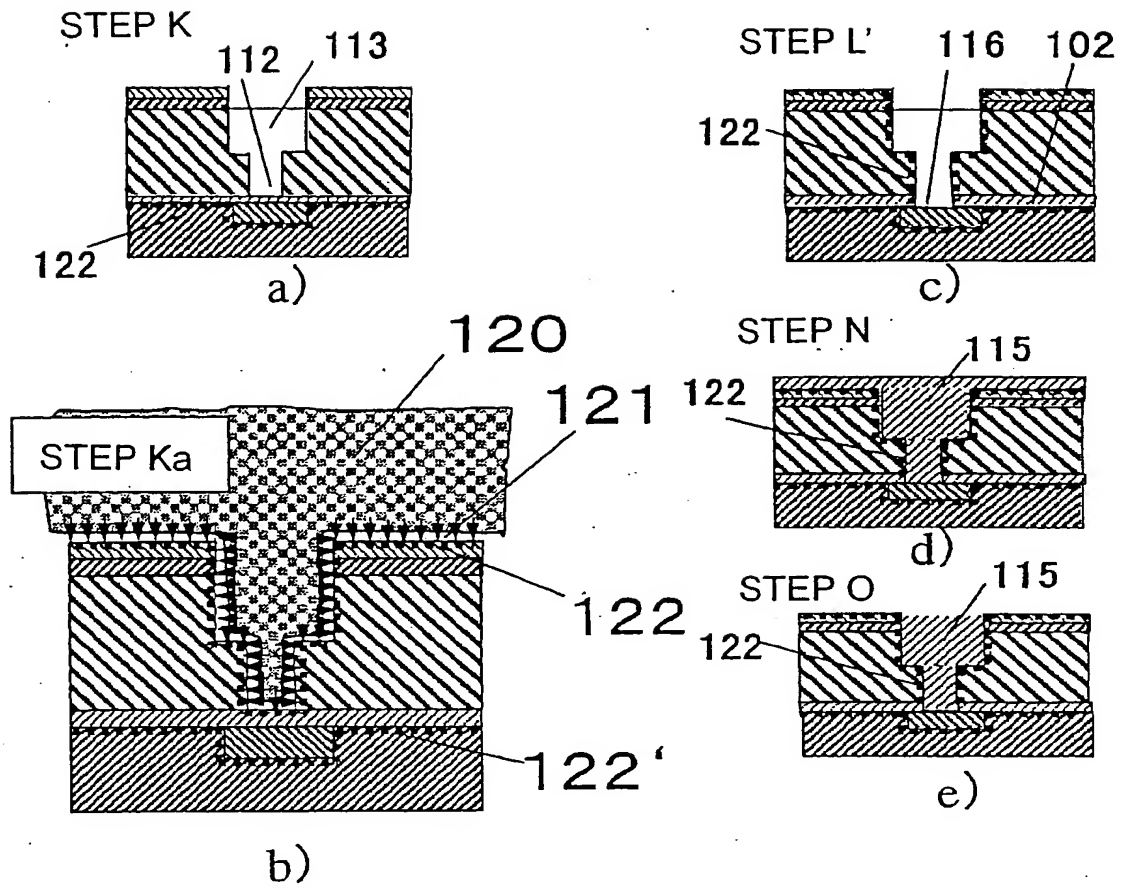


FIG. 4

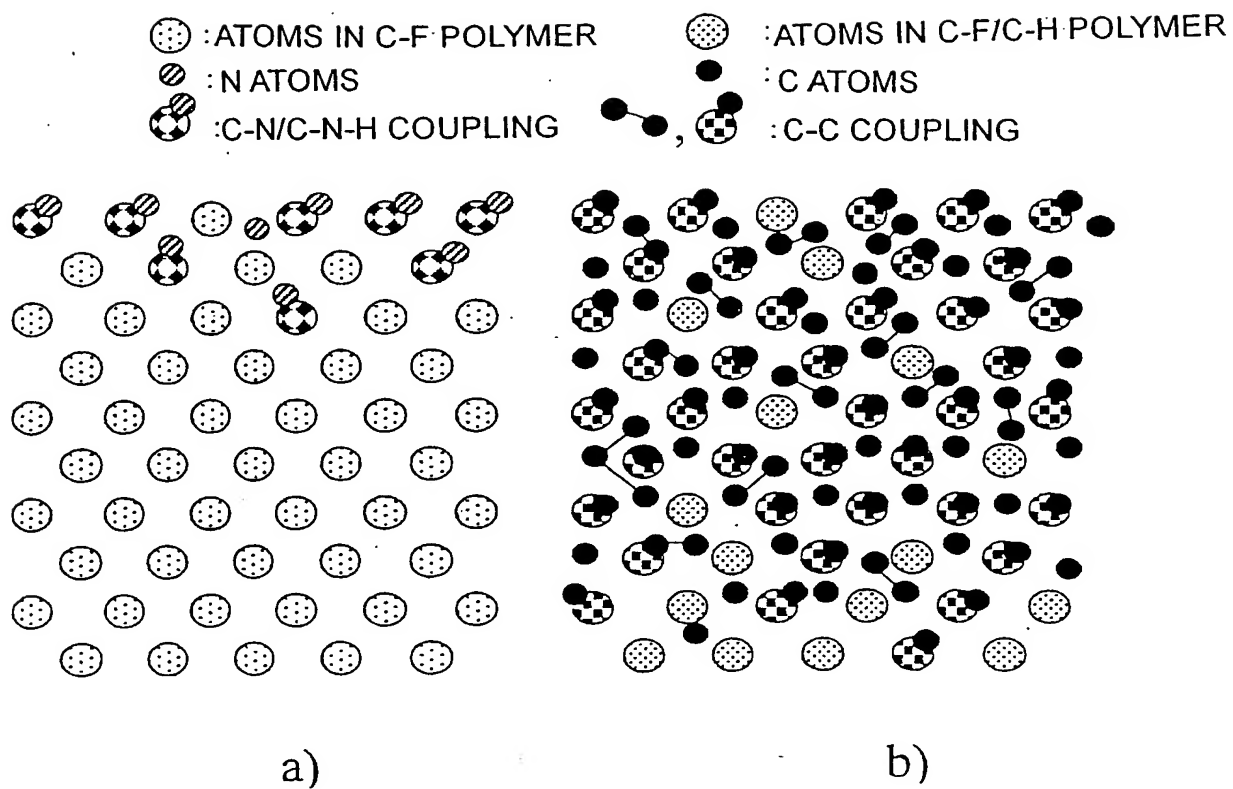


FIG. 5

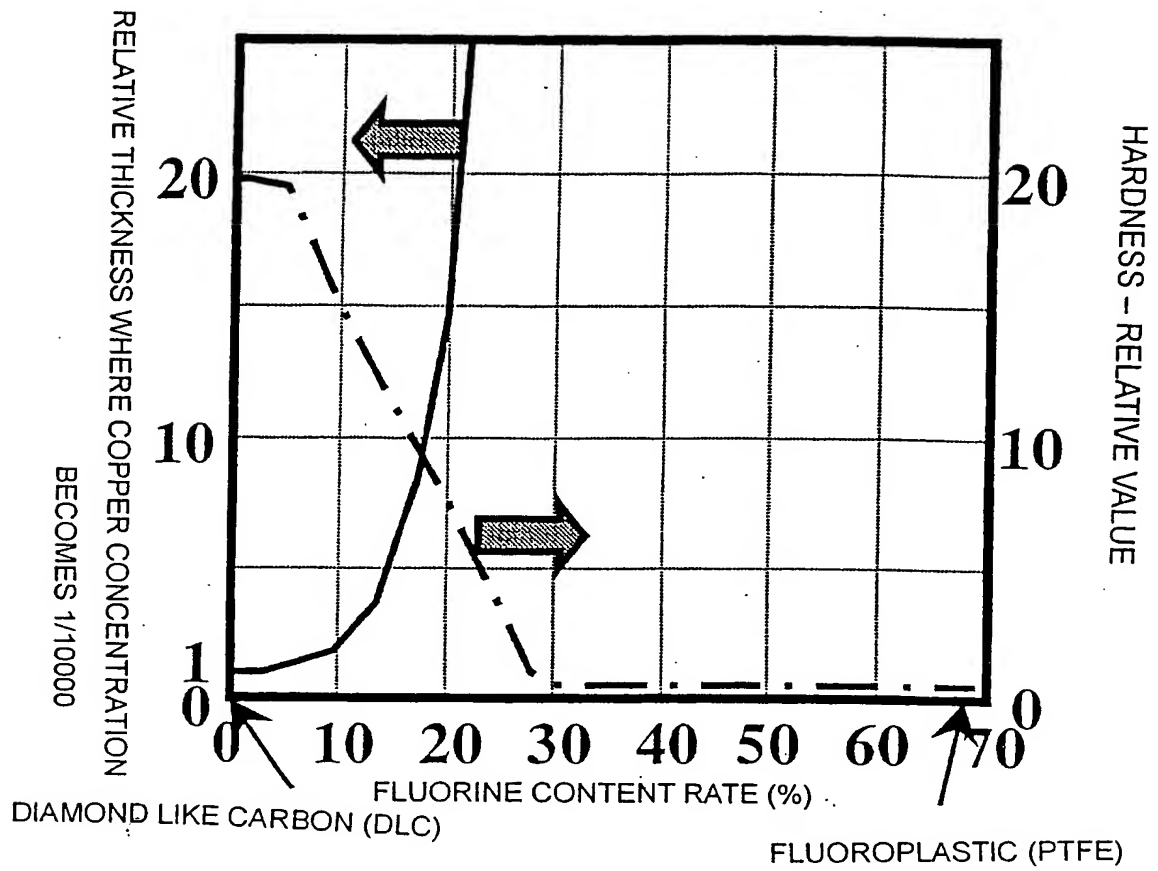
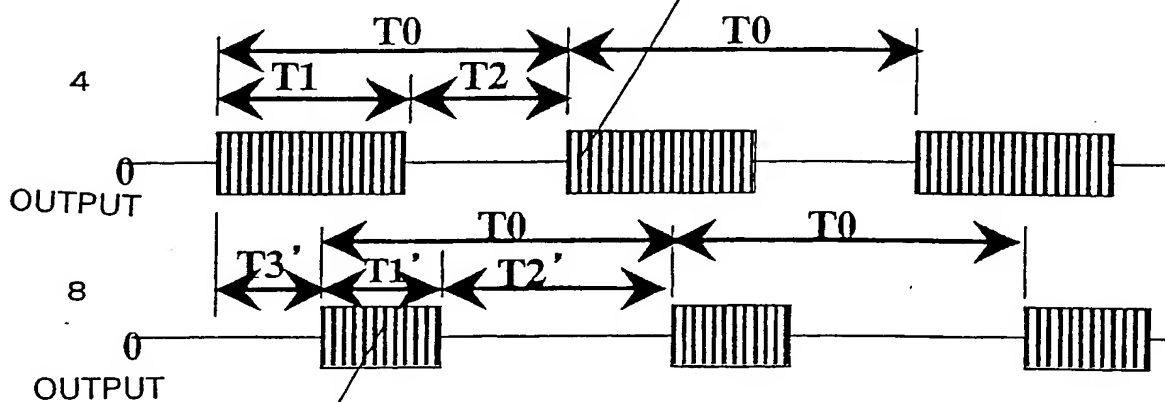


FIG. 6

$$0.2 \leq T_1/T_0 \leq 0.8$$

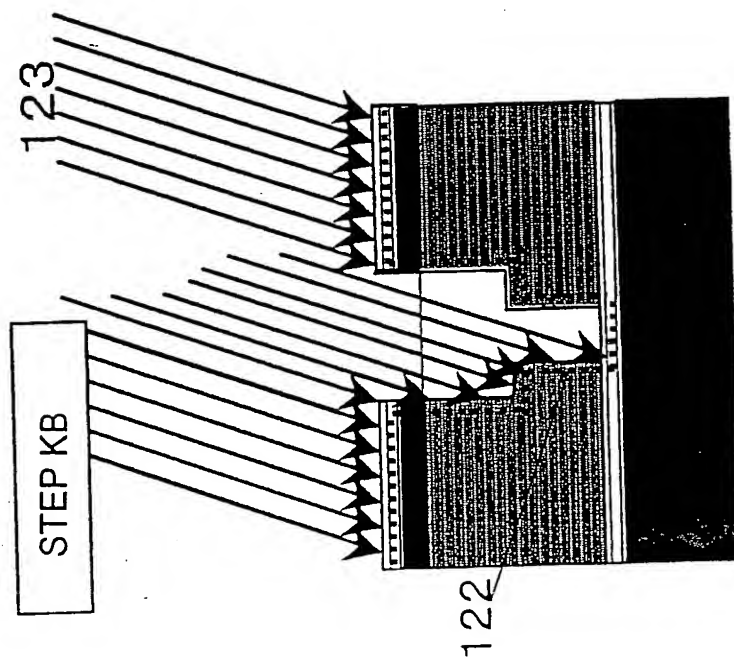
$$10 \leq F_0(\text{MHz}) \leq 2500$$



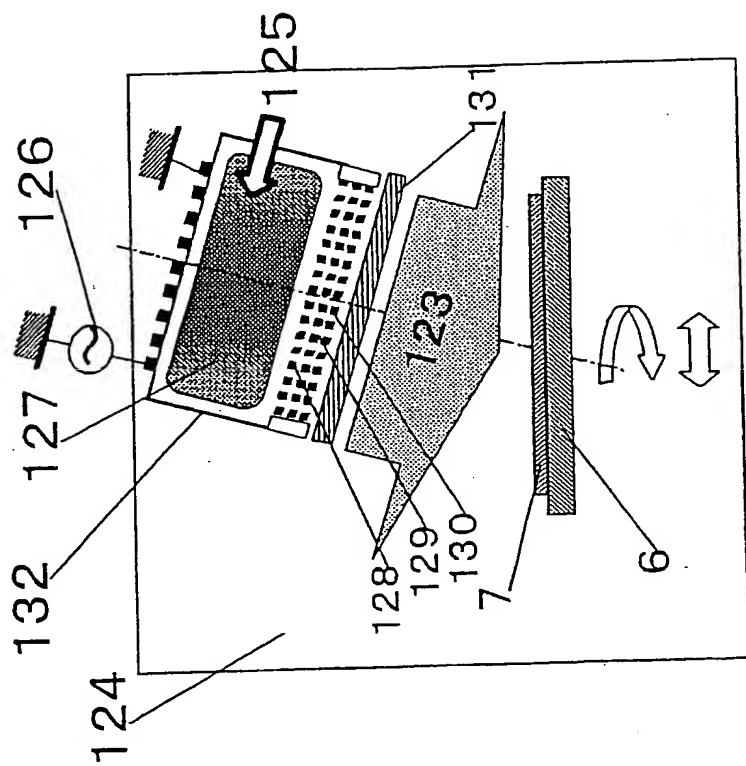
$$0.1 \leq F_1(\text{MHz}) \leq 20 \quad 0 \leq T_3'/T_1 \leq 1$$

$$0.2 \leq T_1'/T_0 \leq 0.8$$

FIG. 7



a)



b)

FIG. 8

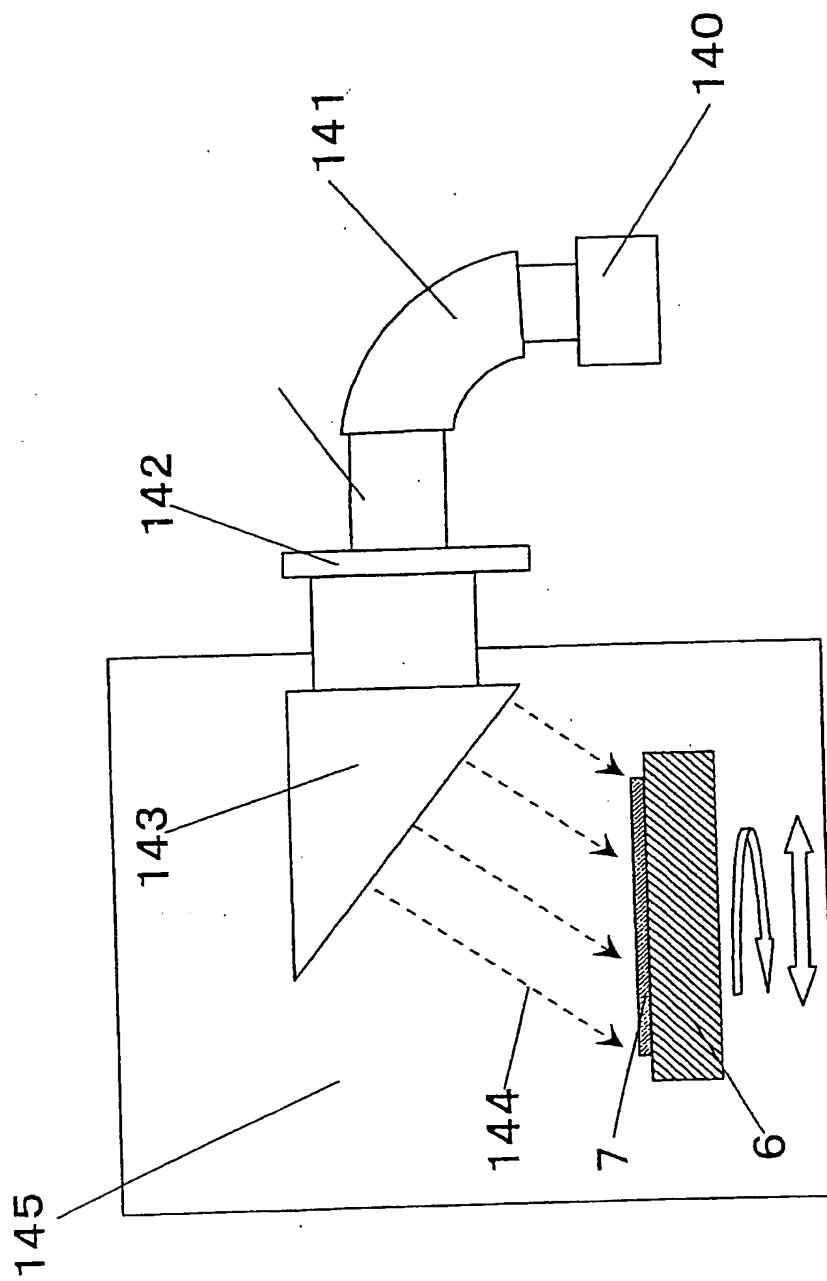


FIG. 9

FIG. 9 is a schematic diagram of a multi-ported device assembly. A central hexagonal component (150) is surrounded by six rectangular ports (151A-151F). Each port is connected to a larger rectangular block (152A-152F) via a thick, shaded ring (153). The blocks are further connected to a large rectangular assembly (154) at the top. This assembly includes two smaller rectangular blocks (158A, 158B) and a central rectangular block (157). The entire assembly is connected to a large rectangular block (145) at the bottom. Various other components and connections are labeled with numbers 155A-156A, 159, 160, 161, 162, and 163.

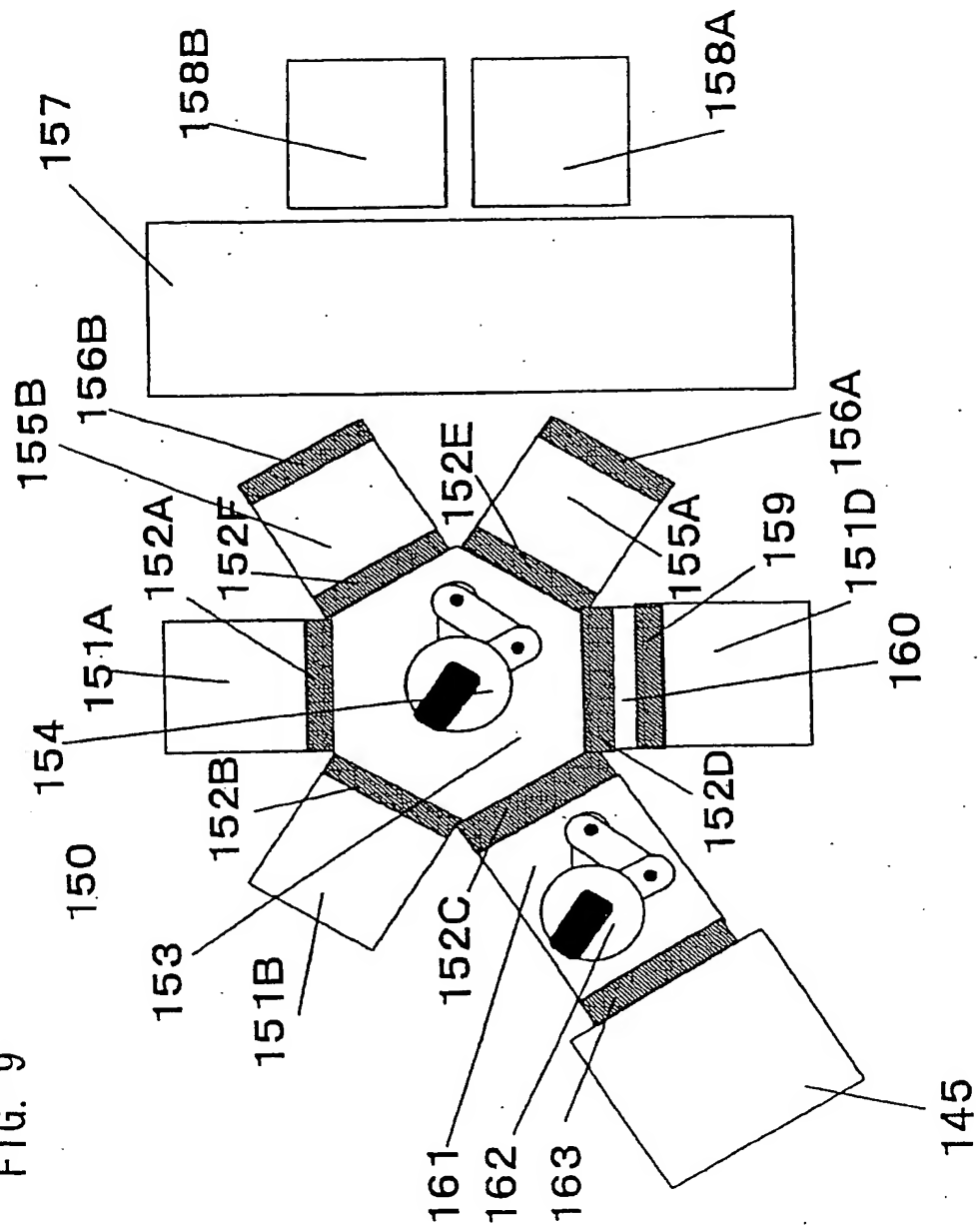


FIG. 10

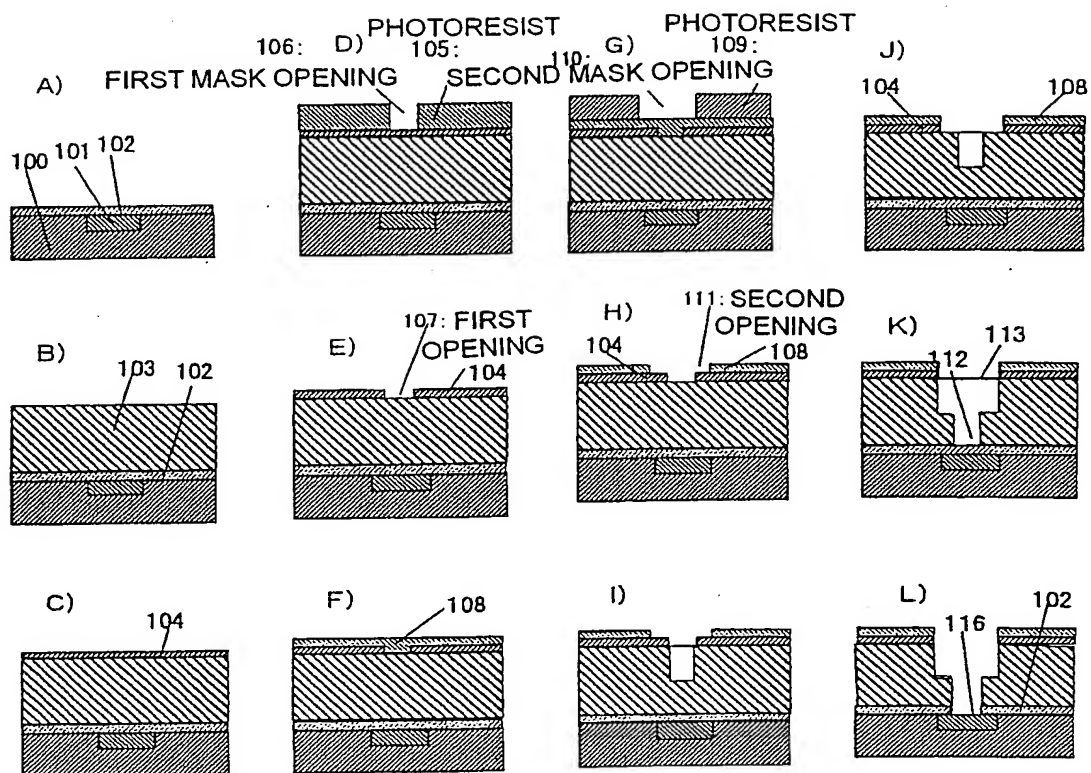


FIG. 11

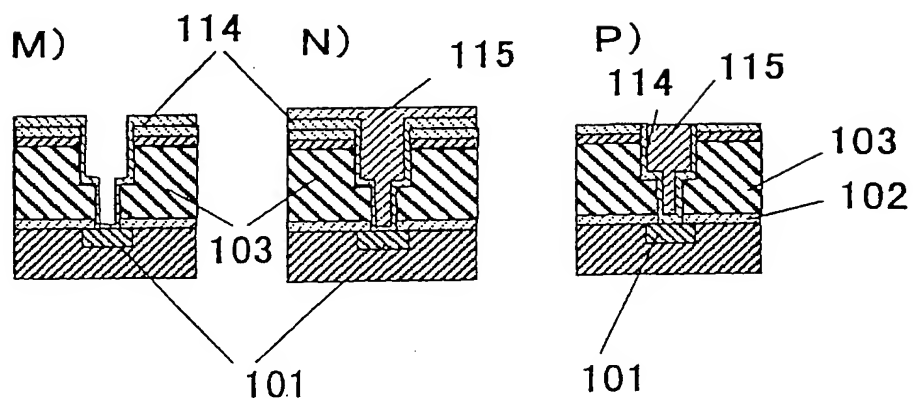


FIG. 12

